EE618
Course Project
Operational Amplifier Design

Autumn 2020

Group 13

Adway Girish 180070002
Anjana Singh 180070008

Contents

Target requirements and specifications

Design an Op-Amp inspired from TI OPA344/345 with the following specifications.

- Single ended output
- Open loop small signal low-frequency voltage gain $> 100\,\mathrm{dB}$
- Unity gain bandwidth $> 10\,\mathrm{MHz}$
- Input CM voltage range: $100\,\mathrm{mV}$ to $1.7\,\mathrm{V}$
- Output voltage range: $100\,\mathrm{mV}$ to $1.7\,\mathrm{V}$
- Phase margin $> 60^\circ$ (Load capacitance $= 5\,\mathrm{pF}$)
- Slew rate $> 2\,\mathrm{V}\,\mu\mathrm{s}^{-1}$ (Load capacitance $= 5\,\mathrm{pF}$)

180 nm Technology parameters

Here are the constant values assumed for 180 nm technology:

$\mu_n C_{ox}$	$300\mu A/V^2$
$\mu_p C_{ox}$	$68\mu A/V^2$
λ_n	$0.1V^{-1}$
λ_p	$0.2V^{-1}$
$\lvert V_{TP}\rvert$	$0.4V$
V_{TN}	$0.4V$

Table 1: Data assumed for 180 nm Technology

1 Design Flow

We start by letting $V_{\text{DSAT,P}} = 0.25\,\text{V}$ and $V_{\text{DSAT,N}} = 0.2\,\text{V}$.

1.1 Iteration 1

1.1.1 Slew Rate

Slew Rate, $\text{SR} > 2\,\text{V}\,\mu\text{s}^{-1}$
$C_C = 4pF$

$$\begin{aligned}\text{SR} = \frac{I_{\text{bias}}}{C_c + C_L} &\geq 2V/\mu s \\ \implies I_{\text{bias}} &\geq 2\,\text{V}\,\mu\text{s}^{-1} \times (4\,\text{pF} + 5\,\text{pF}) = 18\,\mu\text{A} \\ \therefore \text{Take } I_{\text{bias}} &= 40\,\mu\text{A}\end{aligned}$$

From the circuit

$$\begin{aligned}I_{D,19} &= \left(1 + \frac{C_L}{C_C}\right) I_{\text{bias}} = \left(1 + \frac{5}{4}\right) 40\,\mu\text{A} \\ &= 90\mu A \\ &\approx 100\mu A \\ \left(\frac{W}{L}\right)_{19} &= \frac{2I_{D,19}}{\mu_p C_{ox} V_{\text{DSAT,P}}^2} \\ &\approx 42.35\end{aligned}$$

Since the current through M_{19} and M_{20} is the same, we have

$$\begin{aligned}\left(\frac{W}{L}\right)_{20} &= \frac{2I_{\text{D20}}}{\mu_n C_{ox} V_{\text{DSAT,N}}^2} \\ &\approx 15\end{aligned}$$

1.1.2 Unity Gain Bandwidth

Unity Gain Bandwidth, $F_u \geq 10\,\text{MHz}$

$$\begin{aligned}F_u = \frac{g_{m,1}}{2\pi C_c} &\geq 10\,\text{MHz} \\ \implies g_{m,1} &\geq 10\,\text{MHz} \times 2\pi \times 4\,\text{pF} \\ g_{m,1} &\geq 2.51 \times 10^{-4} S\end{aligned}$$

Assuming $g_{m,1} = g_{m,2} = g_{m,3} = g_{m,4}$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{gm_1^2}{2\mu_n C_{ox} I_d}$$
$$\approx 5.25$$
$$\left(\frac{W}{L}\right)_{3,4} = \frac{gm_1^2}{2\mu_p C_{ox} I_d}$$
$$\approx 23.16$$

1.1.3 Phase Margin

Phase Margin, PM $\geq 60^\circ$.
Assuming that $F_u >> P_1$, we have the phase at F_u to be

$$-90^\circ - \tan^{-1}\left(\frac{F_u}{P_2}\right) = -120^\circ$$
$$\implies \tan^{-1}\left(\frac{F_u}{P_2}\right) = 30^\circ$$
$$\therefore P_2 = \sqrt{3}F_u = 17.32\text{MHz}$$

The non dominant pole is given by :-

$$P_2 = \frac{gm_{19}}{2\pi C_L}$$
$$\implies gm_{19} = P_2 \times 2\pi C_L$$
$$= 5.44 \times 10^{-4} S$$

1.1.4 Open loop Gain

Open loop small signal low-frequency voltage gain = 100 dB = 10^5. $A_{v1} \times A_{v2} = 10^5$

$$A_{v2} = (gm_p + gm_n)(r_{op}||r_{on})$$
$$= (gm_{19} + gm_{20})(r_{o19}||r_{o20})$$

Assuming $gm_{19} = gm_{20}$

$$A_{v2} = \frac{2gm_{19}}{(\lambda_p + \lambda_n)I_{D19}}$$
$$= 40.3$$
$$A_{v1} = 10^5/40.3 = 2481.62$$
$$\approx 2500$$

First stage gain (A_{v1})

$$A_{v1} = gm_1 R_{out}$$
$$R_{out} = gm_{10} ro_{10}(ro_8||ro_1)$$
$$A_{v1} = gm_1 gm_{10} ro_{10}(ro_8||ro_1)$$

$$r_{10} = \frac{1}{\lambda_p \times I_{bias}/2} = 250K\Omega \qquad r_1 = \frac{1}{\lambda_n \times I_{bias}/2} = 500K\Omega \qquad r_8 = \frac{1}{\lambda_p \times I_{bias}} = 125K\Omega$$

$$\begin{aligned} gm_{10} &= \frac{A_{v1}}{gm_1 \times ro_{10}(ro_8||ro_1)} \\ &= 2.23 \times 10^{-4} S \\ \left(\frac{W}{L}\right)_{10,9} &= \frac{gm_{10}^2}{2\mu_p C_{ox} I_d} \\ &\approx 58.36 \end{aligned}$$

Assuming $gm_{10} = gm_{16}$

$$\begin{aligned} \left(\frac{W}{L}\right)_{16,15} &= \frac{gm_{10}^2}{2\mu_n C_{ox} I_d} \\ &\approx 13.23 \end{aligned}$$

Assuming current through $M_{7,8,17,18} = 40\mu A$

$$\begin{aligned} \left(\frac{W}{L}\right)_{7,8} &= \frac{2I_D}{\mu_p C_{ox} V_{DSATP}^2} \\ &\approx 18.82 \\ \left(\frac{W}{L}\right)_{17,18} &= \frac{2I_D}{\mu_n C_{ox} V_{DSATN}^2} \\ &\approx 6.67 \end{aligned}$$

When one of the differentials pairs are turn off. Current ($I_{bias}/2$) will flow through either of M_{11}, M_{12}.

$$\begin{aligned} \left(\frac{W}{L}\right)_{11,14} &= \frac{2I_D}{\mu_p C_{ox} V_{DSATP}^2} \\ &\approx 9.41 \\ \left(\frac{W}{L}\right)_{12,13} &= \frac{2I_D}{\mu_n C_{ox} V_{DSATN}^2} \\ &\approx 3.33 \end{aligned}$$

1.1.5 Iteration 1 Results

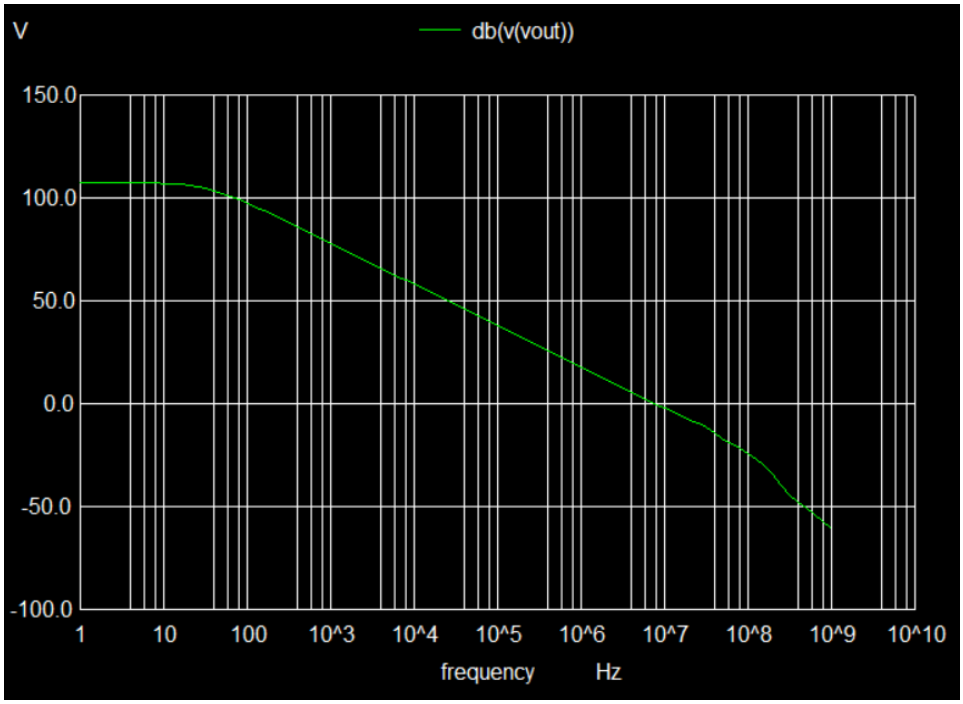


Figure 1: Open loop voltage gain in dB

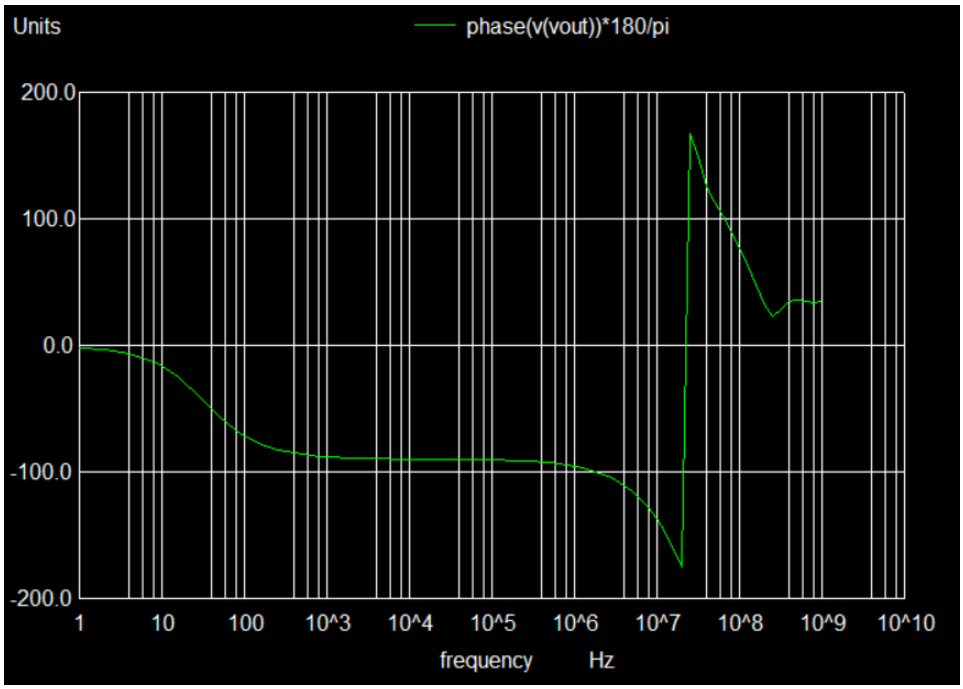


Figure 2: Open loop phase response in degrees

Phase Margin	52.79°
DC gain	107 dB
Unity gain Bandwidth	7.64 MHz

Table 2: Iteration 1 Results

1.2 Iteration 2

To increase Unity gain Bandwidth, we increase gm_1 by increasing W/L of M_1, M_2, M_3, M_4.
As F_u is directly proportional to gm. and gm is proportional to $(W/L)^{0.5}$. We increase W/L by a factor of $(10/7.64)^2 = 1.71$
Therefore, we take $\left(\frac{W}{L}\right)_{1,2} = 12$ and $\left(\frac{W}{L}\right)_{3,4} = 50$
Current phase margin = 52.79°.

$$90 - 52.79 = \tan^{-1}\left(\frac{F_u}{P_2}\right)$$
$$P_2 = 10.23\text{MHz}$$

Required $P_2 = F_u\sqrt{3} = 17.32$ MHz. As the non dominant pole is directly proportional to gm, we increase W/L of M_{19}, M_{20} by a factor of $(17.32/10.23)^2 = 2.87 \approx 3$.
Therefore, $\left(\frac{W}{L}\right)_{19} = 127$ and $\left(\frac{W}{L}\right)_{20} = 45$

1.2.1 Results

Phase Margin	66.04°
DC gain	109.41 dB
Unity gain Bandwidth	10.31 MHz

Table 3: Final Results

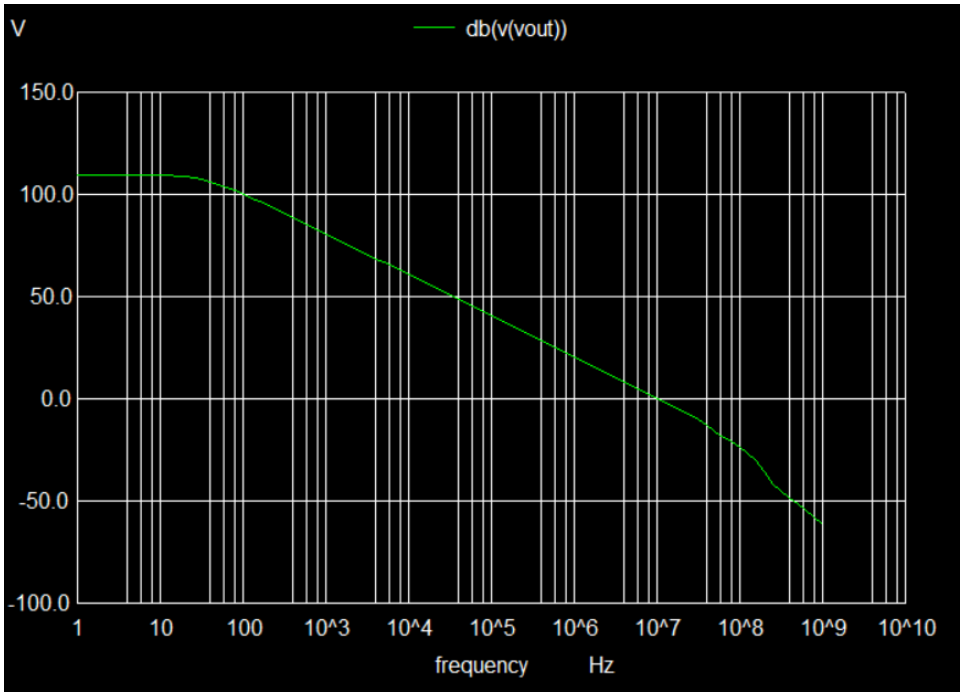


Figure 3: Open loop voltage gain in dB

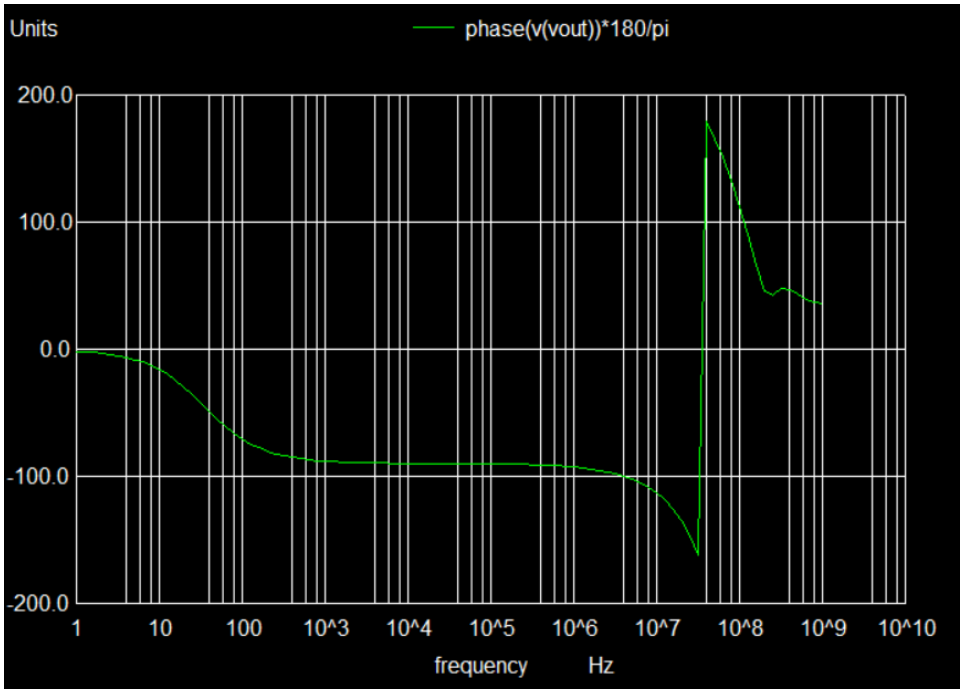


Figure 4: Open loop phase response in degrees

1.3 Bias Currents and Voltages

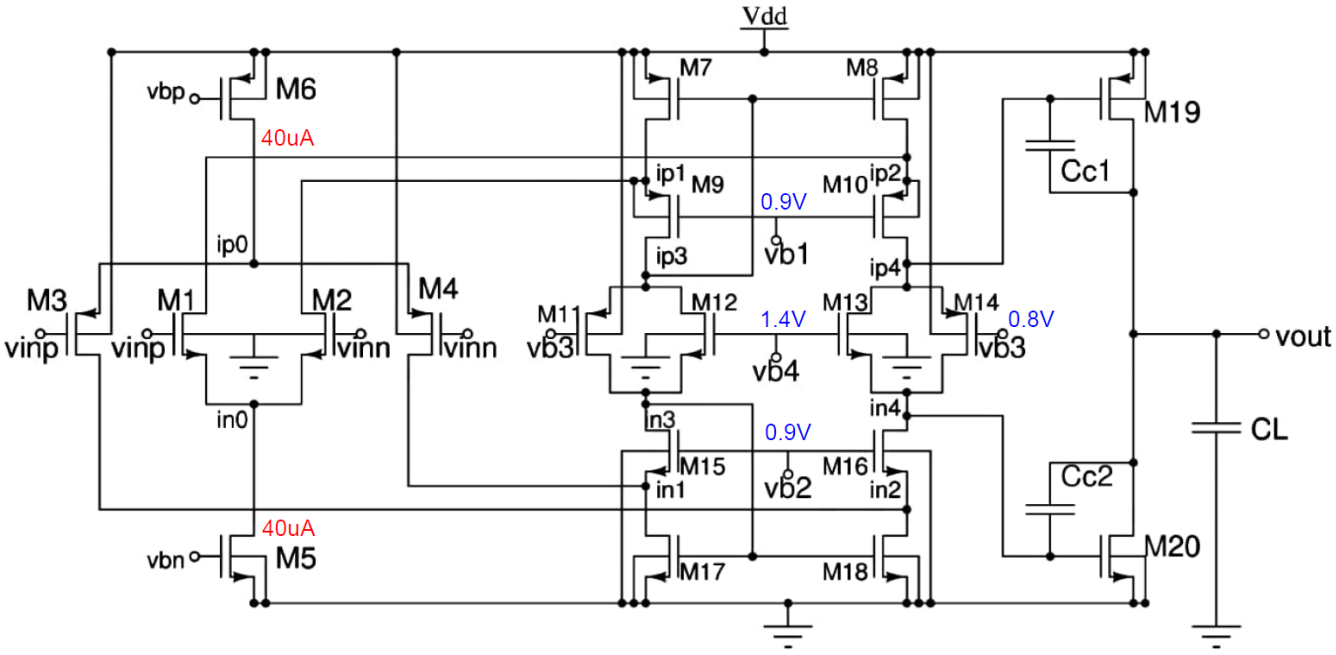


Figure 5: Schematic with Bias Voltages and Current

1.4 Transistor sizes

Mosfet Number	W/L	Mosfet Number	W/L
1	12	11	9.41
2	12	12	3.33
3	50	13	3.33
4	50	14	9.41
5	3	15	13.23
6	15	16	13.23
7	18.82	17	6.67
8	18.82	18	6.67
9	58.36	19	127
10	58.36	20	45

Table 4: Size of MOSFETs

2 Reference Current/Voltage Generation

2.1 Circuit

$I_{bias} = 40\mu A$

$$I_{bias} = \frac{2}{\mu_n C_{ox}(W/L)_N} \frac{1}{R_s^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

Assuming $(W/L)_{38} = 5$ and $K = 5$

$$R_s^2 = \frac{2}{\mu_n C_{ox}(W/L)_N} \frac{1}{I_{bias}} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$
$$R_s = 4K\Omega$$

To keep MOSFETs in saturation,

Bias Voltage	Value
Vb1	0.9
Vb2	0.9
Vb3	0.8
Vb4	1.4

Table 5: Bias Voltages

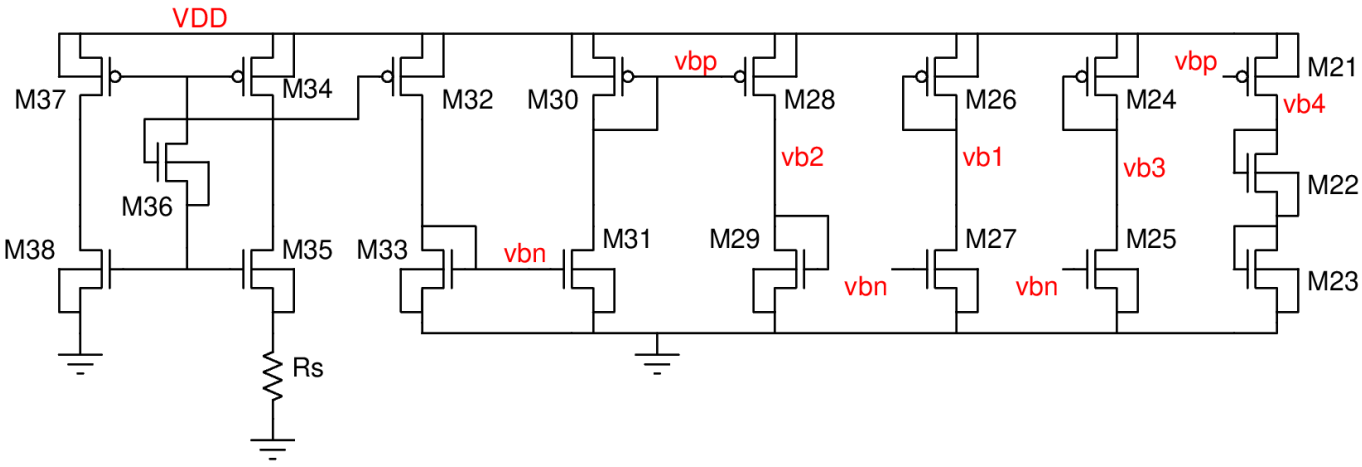


Figure 6: Reference generation design circuit

2.2 Design Procedure

The transistors M34, M35, M36 (startup), M37, M38 are used to generate I_{bias} $(40\mu A)$ as given above.
We took $(W/L)_{34,36,37,38} = 5$. With k=5, we have $(W/L)_{35} = 25$.
The current is mirrored through M32 and M33 is used to generate V_{bn}.
We take $(W/L)_{33,31} = 3$ and $(W/L)_{28,30} = 15$. The current is again mirrored through M28 with M29 as diode connected we calculate $(W/L)_{29}$.

Similarly mirroring and using the values of bias voltages, we find the W/L ratio of the other transistors.

2.3 Transistor Sizes

Mosfet Number	W/L	Mosfet Number	W/L
21	7.5	30	15
22	2.13	31	3
23	2.13	32	5
24	2.5	33	3
25	1.5	34	5
26	3.7	35	25
27	1.5	36	5
28	15	37	5
29	1.7	38	5

Table 6: Size of MOSFETs

3 DC Simulations

Here is the circuit diagram with currents and voltages shown at operating point.

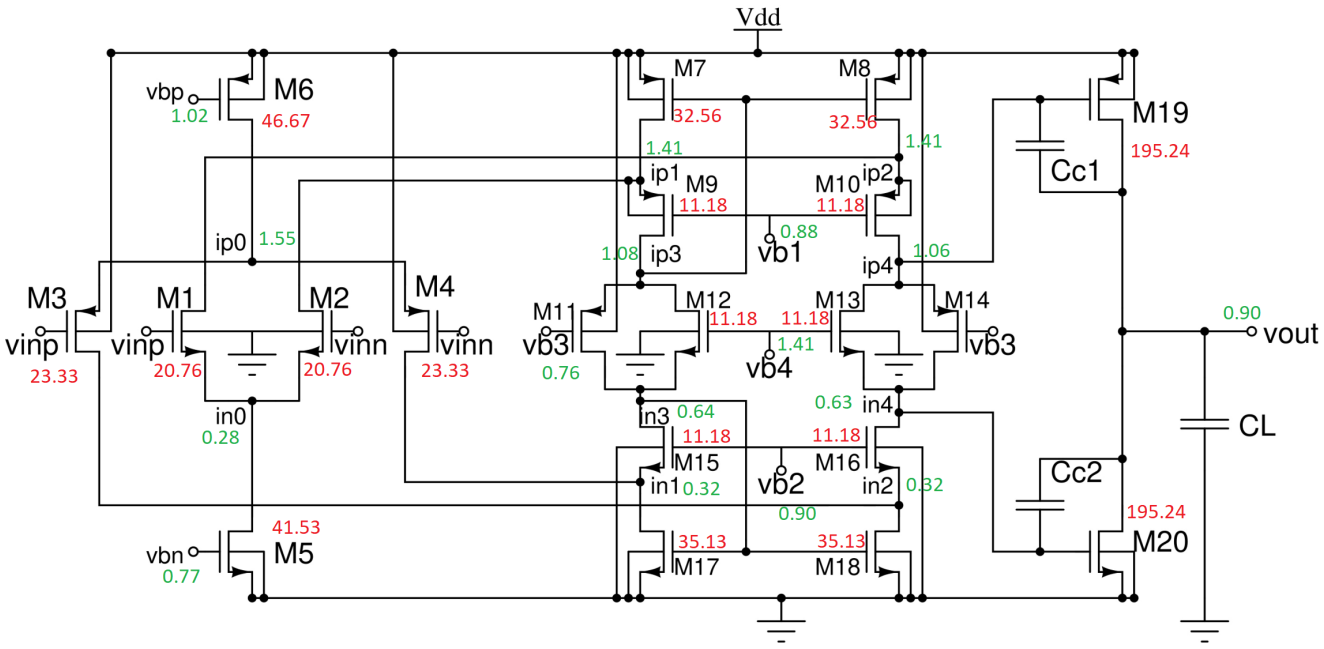


Figure 7: Node voltages (in V, green) and currents (in µA, red)

We see that all transistors except M_{11} and M_{14} are in saturation.

4 AC Simulations

Note : We are ignoring parasitic capacitance as they will be of the order of fF.

We first perform hand calculations to estimate the poles and zeros.

First the dominant pole is given by

$$\begin{aligned}
P_1 &= \frac{1}{2\pi}\frac{1}{(R_1+R_2+G_{m2}R_1R_2)C_2+R_1C_1+R_2C_3} \\
&\approx \frac{1}{2\pi}\frac{1}{G_{m2}R_1R_2C_2} = \frac{1}{2\pi}\frac{1}{C_{C1}|A_{v,2}|R_1} \\
&= \frac{1}{2\pi}\frac{1}{C_{C1}|A_{v,2}|g_{m,10}r_{o,10}r_{o,8}} \\
&= \frac{1}{2\pi}\frac{1}{4\times10^{-12}\times40.3\times2.23\times10^{-4}\times250\times10^{3}\times125\times10^{3}} \\
&= \boxed{1.417\times10^{2}\,\text{Hz}}
\end{aligned}$$

Then we have the non dominant pole, given by

$$\begin{aligned}
P_2 &= \frac{1}{2\pi}\frac{G_{m2}C_2}{C_1C_2+C_1C_3+C_2C_3} \\
&\approx \frac{1}{2\pi}\frac{G_{m2}}{C_3} = \frac{1}{2\pi}\frac{g_{m,19}}{C_L} = \frac{1}{2\pi}\frac{5.44\times10^{-4}}{5\times10^{-12}} \\
&= \boxed{1.732\times10^{7}\,\text{Hz}}
\end{aligned}$$

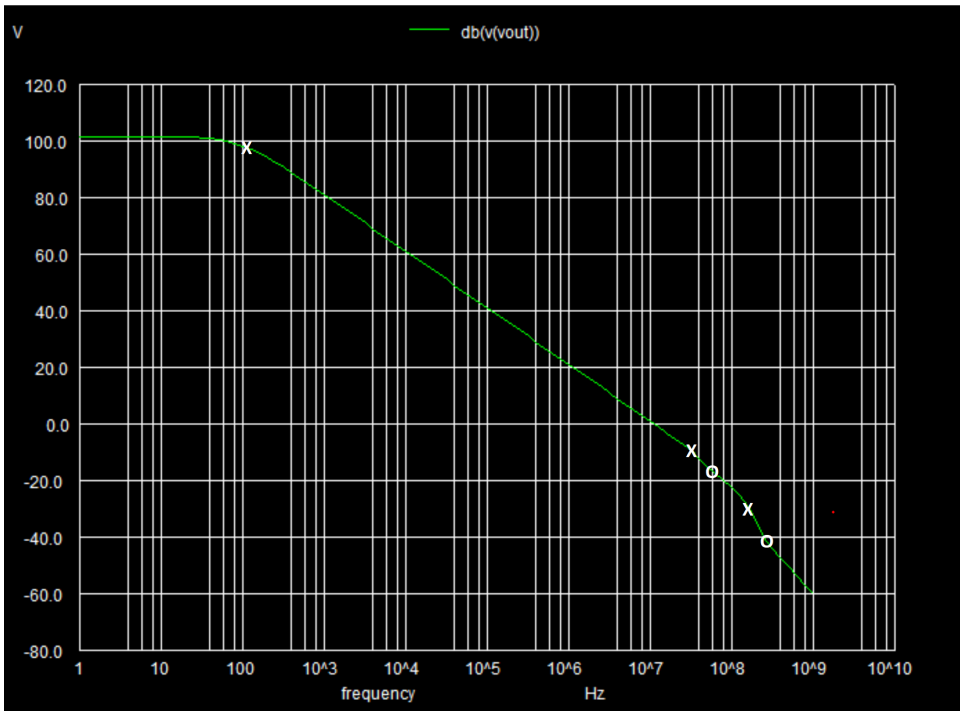
The zero is given by

$$\begin{aligned}
Z_1 &= \frac{1}{2\pi}\frac{g_{m,19}}{C_{C1}} = \frac{1}{2\pi}\frac{5.44\times10^{-4}}{4\times10^{-12}} \\
&= \boxed{2.165\times10^{7}\,\text{Hz}}
\end{aligned}$$

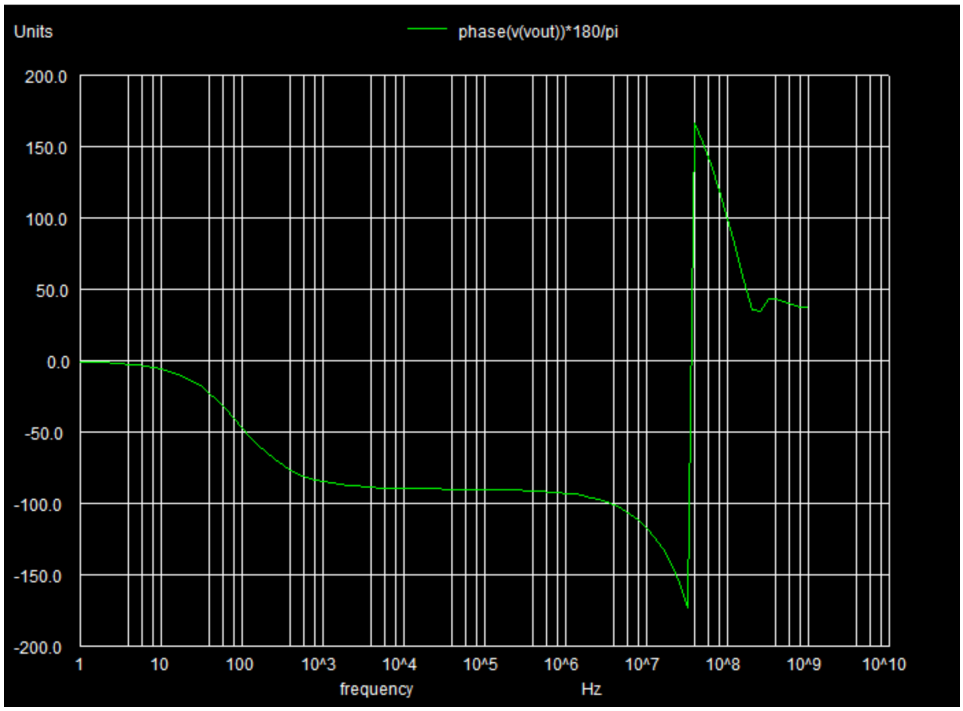
Now we run simulations and obtain the values:
pole(1) = -1.04985e+09,
pole(2) = -5.46599e+08,
pole(3) = -4.86456e+08,
pole(4) = -4.75118e+08,
pole(5) = -4.75118e+08,
pole(6) = -4.16300e+08,
pole(7) = -4.16300e+08,
pole(8) = -1.77794e+08,
pole(9) = $\boxed{\text{-3.03840e+07}}$,
pole(10) = $\boxed{\text{-2.17883e+02}}$,
zero(1) = -7.94640e+08,
zero(2) = -7.94640e+08,
zero(3) = -7.43608e+08,
zero(4) = -5.50337e+08,
zero(5) = -5.50337e+08,

zero(6) = -4.97723e+08,
zero(7) = -1.77794e+08,
zero(8) = $\boxed{\text{-3.17266e+07}}$

We see that pole(10) is the dominant pole, with magnitude = $2.178\,83 \times 10^3$ Hz, pole(9) is the first non dominant pole with magnitude = $3.038\,40 \times 10^7$ Hz, and zero(8) is the dominant zero with magnitude = $3.172\,66 \times 10^7$ Hz, which are all close to our estimated values above.



(a) Open loop differential voltage gain (in dB), showing poles as 'X' and zeros as 'O'



(b) Phase of open loop voltage gain as a function of frequency (in °)

Figure 8: AC Simulations

We get the following values:

DC gain = 109.4118 dB
Unity gain frequency = 1.03×10^7 Hz
Phase Margin = 65.5°
Roll off at one octave above unity gain frequency = 6.09 dB/octave

5 Slew Rate Simulation

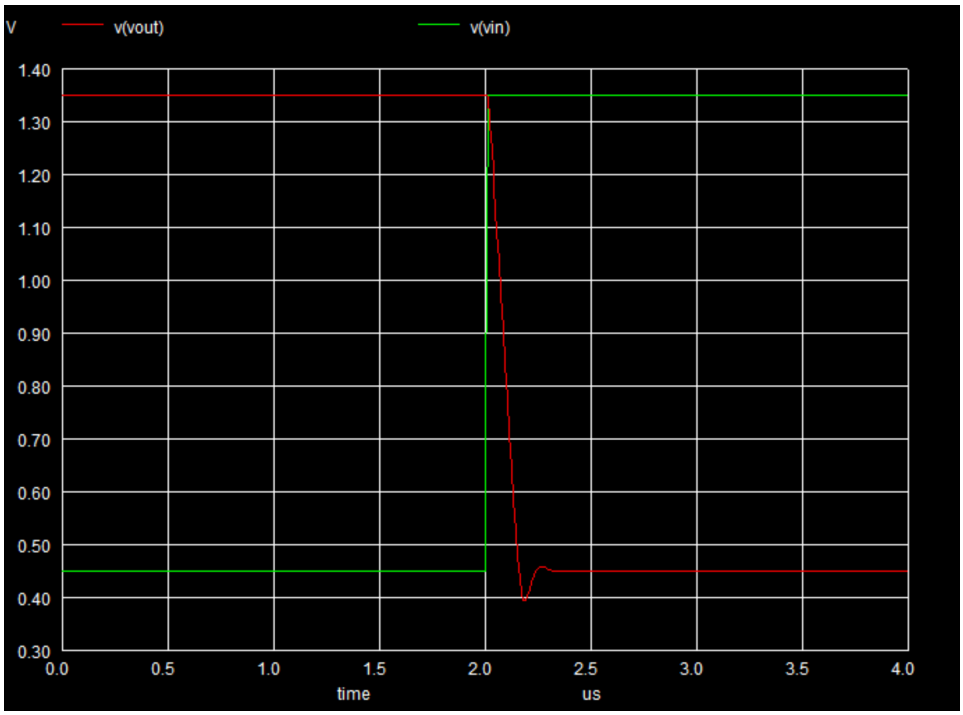


Figure 9: Slew Rate Simulation, with input as a step response (in green) and output (in red)

We measure the maximum value of the magnitude of the slope of V_{out} in Fig. 9, and we get $\boxed{\mathrm{SR} = 6.598\,673\,\mathrm{V}\,\mu\mathrm{s}^{-1}}$.

6 Transient Simulation

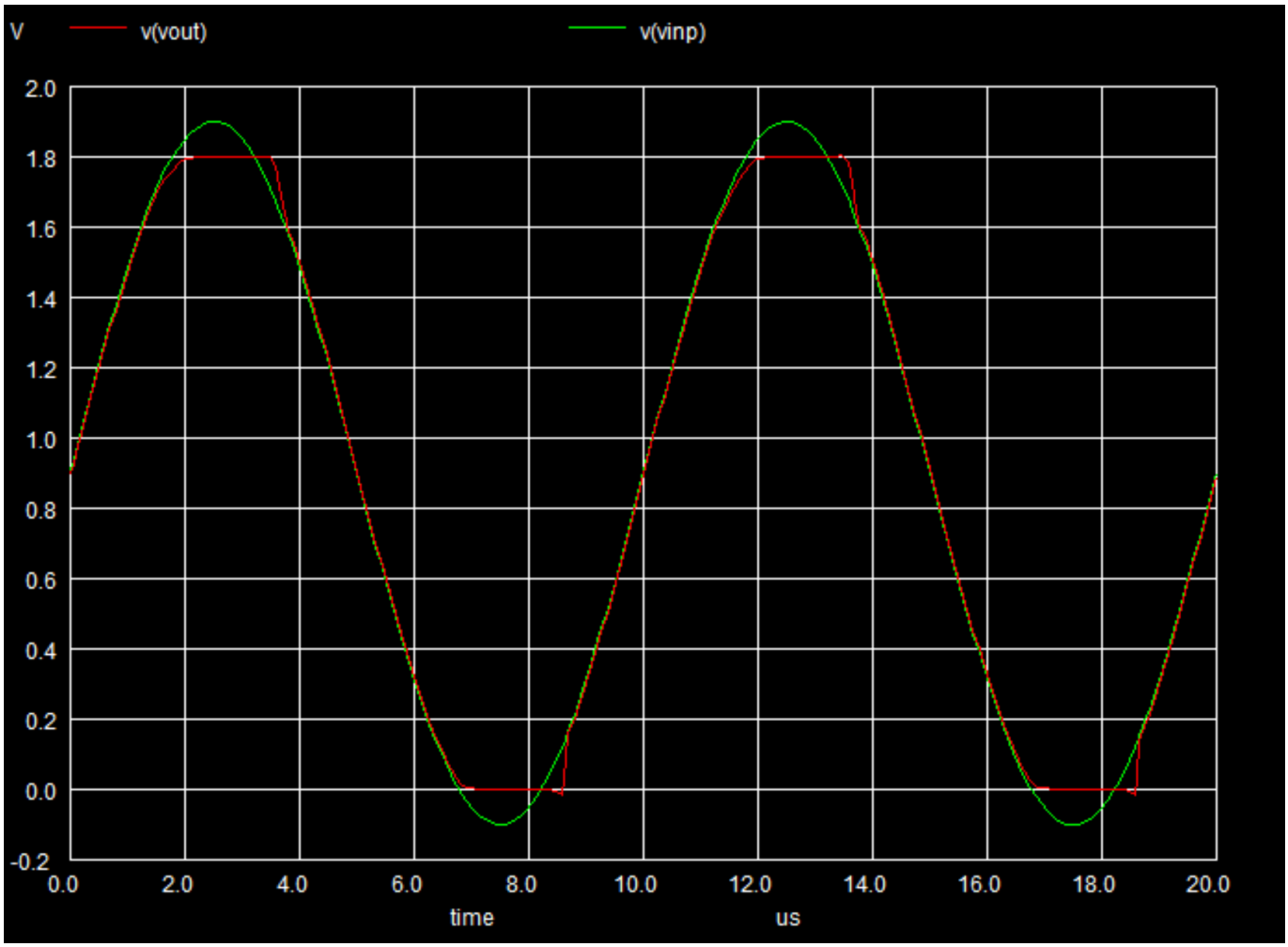
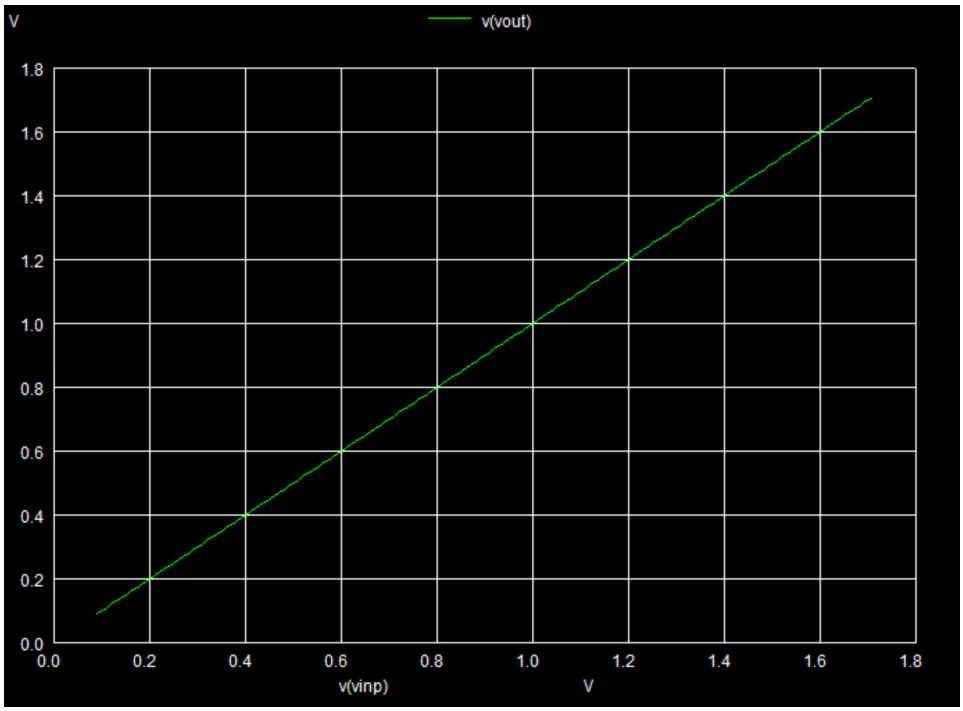


Figure 10: Transient Simulation for maximum output voltage swing

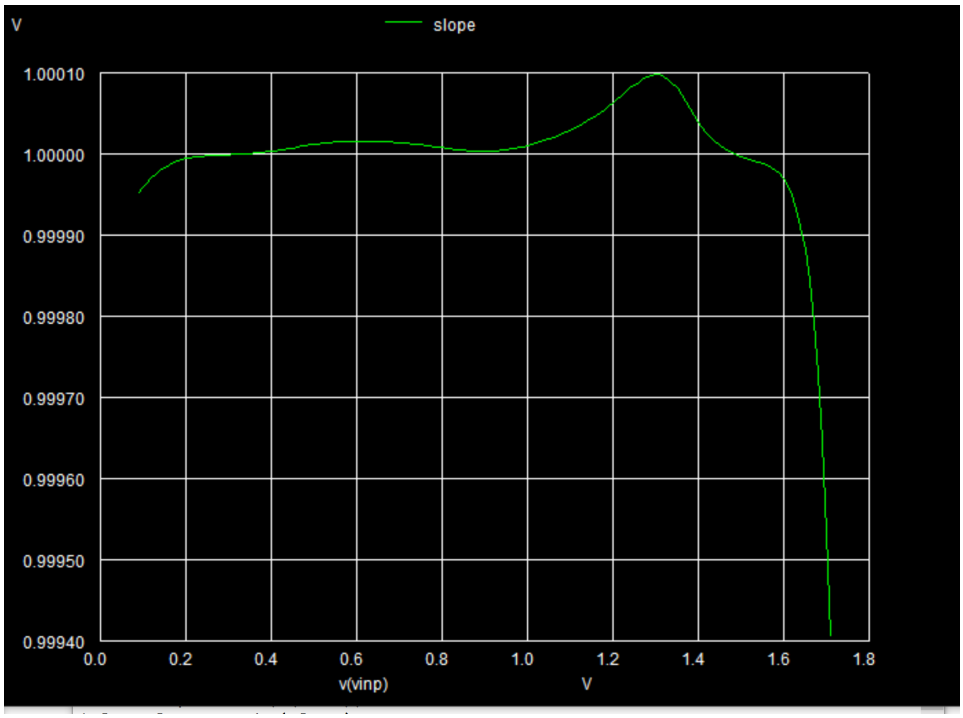
We see that the output voltage saturates between 0 and V_{DD} even as the peak-to-peak input amplitude is greater than 1.8 V. Hence the maximum output voltage swing is from 0 to $V_{DD} = 1.8\,\text{V}$.

7 Common Mode DC Simulation

The plots showing the non-linearity of the opamp are shown in Fig. 11.



(a) Common Mode DC Sweep from $V_{CM,min}$ to $V_{CM,max}$ showing output CM DC voltage as a function of input CM DC voltage



(b) Common Mode DC Sweep from $V_{CM,min}$ to $V_{CM,max}$ showing slope vs V_{CM}

Figure 11: Common Mode DC Simulations

Fig. 11a shows the output CM DC voltage as a function of input CM DC voltage, and we see

that it is almost linear. To see that it is actually non linear, we have Fig. 11b, which shows the slope of the output voltage, and we see that the slope is not exactly 1.

We measure the value of the slope at three points as needed:

V_{CM}	Slope
100 mV	9.999591×10^{-1}
0.9 V	1.000003
1.6 V	9.999692×10^{-1}

Table 7: Non Linearity of Op Amp

The minimum and maximum of the slope values at the three points above are 0.999 959 1 V and 1.000 003 V respectively.

The minimum and maximum of the slope values over the entire range considered are 0.999 549 6 V at 1.7 V and 1.000 098 V at 1.3 V respectively.

8 Work Contribution

Question Number	Adway Girish	Anjana Singh
1.1	(✓) done by both together	(✓) done by both together
1.2	(✓) done by both together	(✓) done by both together
1.3	(✓) done by both together	(✓) done by both together
1.4	(✓) done by both together	(✓) done by both together
2.1		(✓)
2.2		(✓)
2.3		(✓)
3.1		(✓)
3.2		(✓)
3.3		(✓)
4.1	(✓)	
4.2	(✓)	
4.3	(✓)	
4.4	(✓)	
5.1	(✓)	
5.2	(✓)	
6.1		(✓)
6.2		(✓)
7.1	(✓)	
7.2	(✓)	
7.3	(✓)	
7.4	(✓)	

Table 8: Work Contribution